Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **ADJ/GND**
2. **INPUT**
3. **V OUT**
4. **INPUT**
5. **V OUT**
6. **V OUT**

**.084”**

**MASK**

**REF**

**LM1085A ADJ**

**6**

**1**

**5**

**4**

**3**

**2**

**.123”**

**Top Material: Al**

**Backside Material: TiNiAg**

**Bond Pad Size: .004” X .004”**

**Backside Potential: V OUT**

**Mask Ref: LM1085A ADJ**

**APPROVED BY: DK DIE SIZE .084” X .123” DATE: 7/7/22**

**MFG: NATIONAL SEMI THICKNESS .013” P/N: LM1085**

**DG 10.1.2**

#### Rev B, 7/19/02